UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/596,027	06/15/2000	David Charles McClure	95-C-153RE (1678-26)	1327

30431 7590 03/30/2010

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
LE, DINH THANH	
ART UNIT	**PAPER NUMBER**
2816	

NOTIFICATION DATE	DELIVERY MODE
03/30/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

angie.rodriguez@st.com
ip.us@st.com

Supplemental Notice of Allowability	Application No. 09/596,027	Applicant(s) MCCLURE, DAVID CHARLES	
	Examiner Lincoln Donovan	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 08-20-2009*.

2. ☒ The allowed claim(s) is/are *1-18, 20-26 and 28-39*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Lincoln Donovan/
Supervisory Patent Examiner, Art Unit 2816

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Claims:

1. (Original) A method of internally controlling a clock signal of an integrated circuit device such that a data path of the integrated circuit device is initialized in a test mode, comprising the steps of:
upon a power-up condition in the test mode of the integrated circuit device forcing the clock, signal of the integrated circuit device to a first logic state, thereby causing a master element of the integrated circuit device to load in first data and to conduct; and
upon completion of the power-up condition forcing the clock signal of the integrated circuit device to a second logic state, thereby latching in the first data to the master element and causing a slave element of the integrated circuit device to load in second data generated by the master element and to conduct.

2. (Original) The method of claim 1, wherein the first logic state is a low logic state and the second logic state is a high logic state.

3. (Original) The method of claim 1, wherein the power-up condition of the integrated circuit device is controlled by a power-on-reset signal of the integrated circuit device.

4. (Original) The method of claim 3, wherein the power-on-reset signal is an internally generated signal which changes logic state once a threshold value of a positive power supply is passed as the positive power supply rises.
5. (Original) The method of claim 1, wherein the clock signal of the integrated circuit device is an external clock signal of the integrated circuit device or a derivative signal of the external clock signal.

6. (Original) The method of claim 1, wherein the master element of the integrated circuit device is a master latch element and the slave element is a slave latch element.

7. (Original) The method of claim 1, wherein the master element of the integrated circuit device is a master flip-flop element and the slave element is a slave flip-flop element.

8. (Original) The method of claim 1, wherein upon the power-up condition of the integrated circuit device, the clock signal is internally clocked.

9. (Original) The method of claim 1, wherein when the master element is conducting the slave element does not conduct and when the slave element is conducting the master element does not conduct.

10. (Original) The method of claim 1, wherein the test mode is entered upon the power-up condition of the integrated circuit device.

11. (Original) The method of claim 1, wherein the data path is an address path.

12. (Original) The method of claim 1, wherein in the test mode the integrated circuit device is tested at a voltage above a normal operating voltage of the integrated circuit device.

13. (Original) The method of claim 12, wherein the clock signal is tested in both the first logic state and the second logic state at the voltage.

14. (Original) The method of claim 1, wherein the integrated circuit device is a synchronous clocked device.

15. (Original) The method of claim 1, wherein conduction of the master element and conduction of the slave element initializes an address path of the integrated circuit device such that a plurality of columns and a plurality of rows of the integrated circuit device are not selected.

16. (Original) The method of claim 1, wherein conduction of the master element and conduction of the slave element initializes an address path of the integrated circuit device such that a plurality of columns and a plurality of rows

of the integrated circuit device are selected.

17. (Original) The method of claim 16, wherein a plurality of bitlines true of the integrated circuit device are held at a first voltage level and a plurality of bitlines complement of the integrated circuit device are held at a second voltage level.

18. (Previously Presented) A method, comprising:
providing power to an integrated circuit:
loading a first data bit into a master latch and causing the integrated circuit to enter a test mode before the power attains a predetermined level, the master latch being disposed on the integrated circuit; generating a second data bit from the first data bit; latching the first data bit in the master latch; and loading the second data bit into a slave latch that is disposed on the integrated circuit.

19. Cancel claim 19.

20. (Previously Presented) The method of claim 18 wherein, generating the second data bit comprises generating the second data bit equal to the first data bit.

21. (Previously Presented) The method of claim 18 wherein generating the, second data bit comprises generating the second data bit equal to a complement of the first data bit.

22. (Previously Presented) The method of claim 18 wherein generating the second data bit comprises generating the second data bit before and after the power attains the predetermined level.

23. (Previously Presented) The method of claim 18 wherein:
loading the first data bit into the master latch comprises simulating an external clock signal having a first clock state; and
latching the first data bit in the master latch and loading the second data bit into the slave latch comprise simulating the external clock signal having a second clock state.

24. (Previously Presented) The method of claim 18 wherein:
loading the first data bit into the master latch comprises simulating an external

clock signal inside the integrated circuit, the clock signal having a first clock state; and
latching the first data bit in the master latch and loading the second data bit into the slave latch comprise simulating the clock signal having a second clock state.

25. (Previously Presented) A method, comprising:
generating a power-on reset signal having a first reset state when power supplied to an integrated circuit has a predetermined first level causing the integrated circuit to enter a test mode;
generating the power-on reset signal having a second reset state when the power has a second predetermined level:
loading a first data bit into a master latch of the integrated circuit in response to the power-on reset signal having the first state;
generating a second data bit from the first data bit;
storing the first data bit in the master latch in response to the power-on reset signal having the second state; and
loading the second data bit into a slave latch of the integrated circuit in response to the power-on reset signal having the second state.

26. (Previously Presented) The method of claim 25 wherein:
generating the power-on reset signal having the first state comprises generating the power-on reset signal having the first state when an integrated-circuit supply voltage has a first predetermined voltage level; and
generating the power-on reset signal having the second state comprises generating the power-on reset signal having the second state when the supply voltage has a second predetermined voltage level.

27. Cancel claim 27.

28. (Previously Presented) The method of claim 25 wherein generating the second data bit comprises generating the second data bit in response to the power-on reset signal having either the first state or the second state.

29. (Previously Presented) The method of claim 25 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise generating a test signal having a first test state.

30. (Previously Presented) The method of claim 25 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise generating multiple test signals each having a first test state.

31. (Previously Presented) The method of claim 25 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise: generating a test signal having a test state; and simulating an external clock signal having a clock state in response to the test signal having the test state.

32. (Previously Presented) The method of claim 25 wherein:
loading the first data bit into the master latch comprises simulating an external clock signal having a first clock state in response to the power-on reset signal having the first reset state; and
storing the first data bit in the master latch and loading the second data bit into the slave latch comprise, generating a test signal having a test state, and simulating the clock signal having a second clock state in response to the test signal having the test state.

33. (Previously Presented) The method of claim 25 wherein:
loading the first data bit into the master latch comprises,
simulating an external clock signal having a first clock state in response to the power-on reset signal having the first reset state.
generating a test signal having a test state, and
generating the first data bit in response to the test signal; and
storing the first data bit in the master latch and loading the second data bit into the slave latch comprise simulating the clock signal having a second clock state in response to the power-on reset signal having the second reset slate and the test signal having the test state.

34. (Previously Presented) The method of claim 25 wherein:
loading the first data bit into the master latch comprises:
simulating an external clock signal having a first clock state in response to the power-on reset signal having the first reset state,
generating a test signal having a first test state, and
generating the first data bit in response to the test signal; and
storing the first data bit in the master latch and loading the second data bit into the slave latch comprise,
generating the test signal having a second test state, and

simulating the clock signal having a second clock state in response to the power-on reset signal having the second reset state and the test signal having the second test state.

35. (Previously Presented) A method, comprising:
providing power to an integrated circuit;
loading a first data bit into a master latch and causing the integrated circuit to enter a test mode before the power attains a predetermined level, the master latch being disposed on the integrated circuit; latching the first data bit in the master latch; and
loading the first data bit into a slave latch of the integrated circuit.

36. (Previously Presented) The method of claim 35 wherein:
loading the first data bit into the master latch comprises generating a clock signal having a first clock state; and
latching the first data bit in the master latch and loading the first data bit; into the slave latch comprise generating the clock signal having a second clock state.

37. (Previously Presented) The method of claim 35 wherein:
loading the first data bit into the master latch comprises generating a clock signal inside the integrated circuit, the clock signal having a first clock state; and
latching the first data bit in the master latch and loading the first data bit into the slave latch comprise generating the clock signal having a second clock state.

38. (Previously Presented) The method of claim 18 wherein:
latching the first data bit comprises latching the first data bit in the master latch after powering up the integrated circuit; and
loading the second data bit comprises loading the second data bit into the slave latch when the power attains the predetermined level.

39. (Previously Presented) The method of claim 35 wherein:
latching the first data bit comprises latching the first data bit in the master latch when the power attains the predetermined level; and
loadin.g the first data bit into the slave latch comprises loading the first data bit into the slave latch when the power attains the predetermined level.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lincoln Donovan whose telephone number is (571)272-1988. The examiner can normally be reached on M-F from 8:30AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan, can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Lincoln Donovan/

Supervisory Patent Examiner, Art Unit 2816